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EXAMINER	
GERSTL, SHANE F	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,573	SAMRA ET AL.	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 have been examined.

Papers Received

2. Receipt is acknowledged of amendment and application data sheet papers submitted where the papers have been placed on record in the file.

3. The objections to the specification, claims, and declaration have been overcome by the amendment and are herein withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-4, 8-10, 11-16, and 20-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Keller (6,636,959).

6. In regard to claim 1, Keller discloses a method for processing instructions in a superscalar microprocessor (figure 1), comprising:

a. selecting an initial sequence of instructions for inclusion in a trace cache line; [Column 5, lines 43-61, give a line predictor that functions as a trace cache. It is inherent that there will be an initial sequence of instructions in the trace cache at some point since it is filled as shown in column 22, lines 62-column 23, line 2.]

b. determining a set of rename resources needed for said trace cache line on a per-packet basis. [Column 23, lines 22-27 with figure 9 show that a line (or packet) is terminated when a maximum number of destination registers (a rename resource) is reached and that this termination is set so that the maximum number of register renames (a rename capacity) is not exceeded. Thus, the set of rename resources needed for each packet is inherently determined so that it can be checked if the maximum has been reached.]

c. adding one or more provisional instructions to said trace cache line to create a provisional trace cache line; [Column 22, line 62 – column 23, line 2, show that a line predictor entry of instructions is created. This entry is then later added to the line predictor, upon termination, so before such adding is done, the entry is a provisional entry or provisional trace cache line.]

d. repeating said determining step for said provisional trace cache line; [Since, as shown in column 22, line 63 – column 23, line 2, the line is only terminated when a certain condition is met, the determining step must be repeated until a condition is met.]

e. comparing said set of rename resources needed for said provisional trace cache line to a rename capacity; [As described above, the line is terminated when the maximum register renames (rename resources) have been reached. This means that it is inherent that a comparison must have been done to see if the maximum number of register renames would be exceeded by the resources needed so the system knows when to terminate the line or packet. The claim

says nothing about a specific resource capacity, but only states **a** resource capacity, and thus the maximum number of register renames that can be done by the map unit (column 23, lines 22-27) is clearly a rename capacity of this map unit.]

f. and accepting said one or more provisional instructions for inclusion in said trace line and repeating said adding step, or rejecting said one or more provisional instructions, based on said comparing step. [Column 22, line 65 – column 23, line 2, shows that upon termination the entry is written to the line predictor. Thus the line predictor, or trace cache, accepts a provisional cache line.]

7. In regard to claim 2, Keller discloses a method in accordance with claim 1, as described above, wherein: said set of rename resources needed and said rename capacity include a source parameter. [Column 7, lines 22-27, show that the map (rename) unit renames both destination and source registers. Therefore, there is a source parameter of the rename capacity. Figure 9 and column 23, lines 24-27, shows that one of the conditions for line termination is that the maximum number of renames has been reached. Therefore the resources needed would include a source parameter to show such renames.]

8. In regard to claim 3, Keller discloses a method in accordance with claim 1, as described above, wherein: said set of rename resources needed and said rename capacity include a destination parameter. [Column 7, lines 22-27, show that the map (rename) unit renames both destination and source registers. Therefore, there is a

destination parameter of the rename capacity. Figure 9 and column 23, lines 24-27, shows that one of the conditions for line termination is that the maximum number of renames has been reached. Therefore the resources needed would include a destination parameter to show such renames.]

9. In regard to claim 4, Keller discloses a method in accordance with claim 1, wherein: said set of rename resources needed and said rename capacity include a line size parameter. [Figure 9 shows a condition for line termination that includes the maximum number of instructions, which give the line size. Therefore, there is a line size parameter for resources needed and a capacity.]

10. In regard to claim 8, Keller discloses a method in accordance with claim 1, as described above, wherein: selecting said initial sequence of instructions uses a worst case assumption of said set of rename resources needed. [The examiner is taking the worst-case assumption to mean that the trace cache is filled initially with the number of instructions that would be the maximum number of instructions if the maximum number of dependencies were present as noted in the specification. As shown above, column 22, line 62 – column 23, line 2, describes that the line predictor entry is filled until a termination occurs. This means that the number of initially selected instructions in the line will at some point signify a worst case scenario and then will either be terminated or continue to be filled.]

11. In regard to claim 9, Keller discloses a method in accordance with claim 1, as described above, wherein: selecting said initial sequence of instructions includes tabulating a maximum rename resource cumulative total based on a plurality of

instruction types. [As shown above, the number of rename resources needed is determined. This can be seen as tabulating a total because as shown, instructions are added based on resource availability until a maximum is reached, so a count must be kept to compare to the capacity. Once the line is filled, this total shows the maximum for that line. Keller's disclosure allows for multiple instruction types as shown throughout.]

12. In regard to claim 10, Keller discloses a method in accordance with claim 1, as described above, wherein: selecting a number of provisional instructions is performed based on a difference between said set of rename resources needed and said rename capacity. [As shown above, instructions are added to the provisional line until a termination condition is encountered. These conditions include maximum the number of renames. Also as shown, the number of resources needed is determined and compared to the capacity. If there is a difference, the capacity has not been reached, and instructions are added. Thus the number of provisional instructions chosen, zero or another number, is based on the difference between resources needed and capacity.]

13. In regard to claim 11, Keller discloses an apparatus for processing instructions in a superscalar microprocessor (figure 1), comprising:

a. an instruction stream with a plurality of instructions (column 2, line 30);

b. a trace cache line to receive said instructions from said instructions stream; [Column 5, lines 59-61 shows a line predictor which acts as a trace cache.]

c. a packetized instruction resource calculator to determine a set of rename resources needed for said instructions in said trace cache line; [Column 23, lines 22-27 with figure 9 show that a line (or packet) is terminated when a maximum number of destination registers (a rename resource) is reached and that this termination is set so that the maximum number of register renames (a rename capacity) is not exceeded. Thus, the set of rename resources needed for each cache line is inherently determined so that it can be checked if the maximum has been reached.]

d. an instruction adder, responsive to said packetized instruction resource calculator, to add one or more instructions to said trace cache line from said instruction stream while said set of rename resources needed is less than a rename resource capacity. [Column 22, line 62 – column 23, line 2 shows that when a line is terminated, it is added to the line predictor, or trace cache. It is also shown that a line is terminated only on a condition given in figure 9. Thus, the line must be examined and added to as long as a condition is not met.]

14. In regard to claim 12, Keller discloses an apparatus in accordance with claim 11, as described above, wherein: said set of rename resources needed includes a source parameter. [Column 7, lines 22-27, show that the map (rename) unit renames both destination and source registers. Therefore, there is a source parameter of the rename capacity. Figure 9 and column 23, lines 24-27, shows that one of the conditions for line termination is that the maximum number of renames has been reached. Therefore the resources needed would include a source parameter to show such renames.]

15. In regard to claim 13, Keller discloses an apparatus in accordance with claim 12, as described above, wherein: said set of rename resources needed and said rename capacity include a destination parameter. [Column 7, lines 22-27, show that the map (rename) unit renames both destination and source registers. Therefore, there is a destination parameter of the rename capacity. Figure 9 and column 23, lines 24-27, shows that one of the conditions for line termination is that the maximum number of renames has been reached. Therefore the resources needed would include a destination parameter to show such renames.]

16. In regard to claim 14, Keller discloses an apparatus in accordance with claim 11, wherein: said set of rename resources needed and said rename capacity include a line size parameter. [Figure 9 shows a condition for line termination that includes the maximum number of instructions, which give the line size. Therefore, there is a line size parameter for resources needed and a capacity.]

17. In regard to claim 15, Keller discloses an apparatus in accordance with claim 14, as described above, wherein: said set of rename resources needed includes a source parameter. [Column 7, lines 22-27, show that the map (rename) unit renames both destination and source registers. Therefore, there is a source parameter of the rename capacity. Figure 9 and column 23, lines 24-27, shows that one of the conditions for line termination is that the maximum number of renames has been reached. Therefore the resources needed would include a source parameter to show such renames.]

18. In regard to claim 16, Keller discloses an apparatus in accordance with claim 15, as described above, wherein: said set of rename resources needed and said rename

capacity include a destination parameter. [Column 7, lines 22-27, show that the map (rename) unit renames both destination and source registers. Therefore, there is a destination parameter of the rename capacity. Figure 9 and column 23, lines 24-27, shows that one of the conditions for line termination is that the maximum number of renames has been reached. Therefore the resources needed would include a destination parameter to show such renames.]

19. In regard to claim 20, Keller discloses an apparatus in accordance with claim 11, as described above, wherein: said trace cache line is loaded with an initial number of instructions. [It is inherent that there will be an initial sequence of instructions in the trace cache at some point.]

20. In regard to claim 21, Keller discloses an apparatus in accordance with claim 20, as described above, wherein: said initial number of instructions is calculated as a fraction of said rename resource capacity. [The examiner is taking the definition of a fraction to be a quotient of two quantities. Therefore, taking the initial number of instructions over said resource capacity will always be calculated as a fraction.]

21. In regard to claim 22, Keller discloses a method of creating cache lines of instructions in a computer system, comprising:

a. determining the number of instructions in the cache lines using a packetization of instructions technique and a dynamic cache line size; [Column 5, lines 59-61 shows a line predictor which acts as a trace cache. Column 22, line 62 – column 23, line 2 shows that a line is terminated on a condition (and thus the size will vary or be dynamic depending on the type and time of a condition).

As shown in figure 9, there is a condition for when a maximum number of renames has been met. Thus in order to see if the condition of the maximum number has been met, the number of instructions that need to be renamed in the cache lines must be determined. Column 22, line 62 – column 23, line 2 also shows that instructions are added to the line predictor, or trace cache, when not terminated. Thus instructions are packed into the line.]

b. matching said dynamic cache line size to a rename unit capacity. [As described above, the line is terminated when the maximum register renames (rename resources) have been reached. This means that it is inherent that a comparison must have been done to see if the maximum number of register renames would be exceeded by the resources needed so the system knows when to terminate the line or packet. The claim says nothing about a specific resource capacity, but only states **a** resource capacity, and thus the maximum number of register renames that can be done by the map unit (column 23, lines 22-27) is clearly a rename capacity of this map unit.]

Claim Rejections - 35 USC § 103

22. Claims 5-7, 17-19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Keller in view of Moudgill.

23. In regard to claim 5,

a. Keller discloses a method in accordance with claim 3, as described above, wherein: determining a set of rename resources needed on a per packet basis.

[Keller has shown as described above that the line of instructions (a packet of instructions) has resources calculated for renaming.]

b. Keller does not disclose that determining rename resources excludes destinations subsequently over-written within the packet from said set of rename resources needed.

c. Moudgill has disclosed that determining rename resources excludes destinations subsequently over-written within the packet from said set of rename resources needed. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that since destination r1 of line 1 is overwritten in line 3, the register r1 does not need to be renamed and thus it is determined that no rename resources are allocated for it.

d. It can easily be seen that by not renaming r1 of line 1, an additional register is not occupied, or it is saved, and can be used for later operations increasing flexibility. This flexibility would have motivated one of ordinary skill in the art to modify the design of Keller to determine the rename resources in the case of overwritten destinations as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to determine rename resources excluding destinations subsequently overwritten within a packet of instructions as taught by Moudgill so that registers are saved allowing for more flexibility.

24. In regard to claim 6,

a. Keller discloses a method in accordance with claim 2, as described above, wherein: determining a set of rename resources needed on a per packet basis. [Keller has shown as described above that the line of instructions (a packet of instructions) has resources calculated for renaming.]

b. Keller does not disclose that determining rename resources excludes redundant sources within the packet from said set of rename resources needed.

c. Moudgill has disclosed that determining rename resources excludes redundant sources within the packet from said set of rename resources needed. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that source r3 of lines 1 and 2 are redundant sources because they refer to the same data. One can also see that these sources are not renamed. Thus it is determined that no rename resources are allocated for them.

d. It can easily be seen that by not renaming r3, additional registers are not occupied, or are saved, and can be used for later operations increasing flexibility. This flexibility would have motivated one of ordinary skill in the art to modify the design of Keller to determine the rename resources in the case of redundant sources as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to determine rename resources excluding redundant sources within a packet of instructions as taught by Moudgill so that registers are saved allowing for more flexibility.

25. In regard to claim 7,

a. Keller discloses a method in accordance with claim 2, as described above, wherein: determining a set of rename resources needed on a per packet basis. [Keller has shown as described above that the line of instructions (a packet of instructions) has resources calculated for renaming.]

b. Keller does not disclose that determining rename resources excludes sources created within said trace cache line.

c. Moudgill has disclosed that determining rename resources excludes sources created within said trace cache line. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that source r1 is changed to source r9 in line 4 and therefore created in the cache line. One can also see that this source does not need a new register allocated to it, because the register has already been renamed in line 3 as the source there. Simply a designation for this register must be assigned. Thus it is determined that no rename resources are allocated for this source.

d. It can easily be seen that by not allocating rename resources for the source r9, additional hardware is saved. This savings in hardware would have motivated one of ordinary skill in the art to modify the design of Keller to determine the rename resources in the case of sources created within the trace cache line (packet) as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to determine rename resources excluding sources created

within the trace cache line (packet) as taught by Moudgill so that registers are saved allowing for more flexibility.

26. In regard to claim 17,

a. Keller discloses an apparatus in accordance with claim 13, as described above.

b. Keller does not disclose wherein: said packetized instruction resource calculator excludes destinations subsequently over-written within said trace cache line from said set of resources needed.

c. Moudgill has disclosed that said packetized instruction resource calculator excludes destinations subsequently over-written within said trace cache line from said set of resources needed. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that since destination r1 of line 1 is overwritten in line 3, the register r1 does not need to be renamed and thus it is determined that no rename resources are allocated for it.

d. It can easily be seen that by not renaming r1 of line 1, an additional register is not occupied, or it is saved, and can be used for later operations increasing flexibility. This flexibility would have motivated one of ordinary skill in the art to modify the design of Keller to determine the rename resources in the case of overwritten destinations as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to determine rename resources excluding destinations

subsequently overwritten within a packet of instructions as taught by Moudgill so that registers are saved allowing for more flexibility.

27. In regard to claim 18,

a. Keller discloses a method in accordance with claim 17, as described above.

b. Keller does not disclose wherein: said packetized instruction resource calculator excludes redundant sources with said trace cache line from said set of resources needed..

c. Moudgill has disclosed that said packetized instruction resource calculator excludes redundant sources with said trace cache line from said set of resources needed. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that source r3 of lines 1 and 2 are redundant sources because they refer to the same data. One can also see that these sources are not renamed. Thus it is determined that no rename resources are allocated for them.

d. It can easily be seen that by not renaming r3, additional registers are not occupied, or are saved, and can be used for later operations increasing flexibility. This flexibility would have motivated one of ordinary skill in the art to modify the design of Keller to determine the rename resources in the case of redundant sources as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to determine rename resources excluding redundant

sources within a packet of instructions as taught by Moudgill so that registers are saved allowing for more flexibility.

28. In regard to claim 19,

a. Keller discloses a method in accordance with claim 18, as described above.

b. Keller does not disclose wherein: said packetized instruction resource calculator excludes sources created within said trace cache line.

c. Moudgill has disclosed that said packetized instruction resource calculator excludes sources created within said trace cache line. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that source r1 is changed to source r9 in line 4 and therefore created in the cache line. One can also see that this source does not need a new register allocated to it, because the register has already been renamed in line 3 as the source there. Simply a designation for this register must be assigned. Thus it is determined that no rename resources are allocated for this source.

d. It can easily be seen that by not allocating rename resources for the source r9, additional hardware is saved. This savings in hardware would have motivated one of ordinary skill in the art to modify the design of Keller to determine the rename resources in the case of sources created within the trace cache line (packet) as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to determine rename resources excluding sources created

within the trace cache line (packet) as taught by Moudgill so that registers are saved allowing for more flexibility.

29. In regard to claim 23,

a. Keller discloses a method in accordance with claim 22, as described above.

b. Keller does not disclose wherein: matching said dynamic cache line size includes eliminating redundant register references within the cache lines.

c. Moudgill has disclosed that matching said dynamic cache line size includes eliminating redundant register references within the cache lines. Figure 1 shows a set of instructions (a) and a renamed set of instructions (b). One can see that source r3 of lines 1 and 2 are redundant sources because they refer to the same data. One can also see that these sources are not renamed. Thus it is determined that no rename resources are allocated for them and thus the line eliminates these sources from updating the line size, which indicates the number of renames.

d. It can easily be seen that by not renaming r3, additional registers are not occupied, or are saved, and can be used for later operations increasing flexibility. This flexibility would have motivated one of ordinary skill in the art to modify the design of Keller to eliminating redundant register references as taught by Moudgill.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Keller to eliminating redundant register references as taught by Moudgill so that registers are saved allowing for more flexibility.

Response to Arguments

30. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

31. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:30-4:00 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
February 3, 2005

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